REMARKS

I. Introduction

Applicants would like to thank Examiner Mai for the indication of allowable subject matter recited by claims 4 and 5. In response to the Office Action dated September 21, 2004, Applicants have amended the title of the invention so as to further describe the present invention. Applicants have canceled claims 1-2 and 6-8, without prejudice or disclaimer. Also, Applicants have amended claim 3 so as to further clarify the claimed subject matter. New claim 9 is added. Support for these amendments can be found, for example, in Figs 3 and 5, and at page 13, line 24 to page 14, line 5 and page 17, line 16 to page 18, line 6 of the specification. No new matter has been added.

For the reasons set forth below, Applicants respectfully submit that all pending claims are patentable over the cited prior art references.

II. The Rejection Of Claim 6 Under 35 U.S.C. § 112, Second Paragraph

Claim 6 is rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. In response, Applicants have canceled claim 6, without prejudice or disclaimer. Thus, the pending rejection to claim 6 under 35 U.S.C. § 112, second paragraph is moot.

III. The Rejection Of Claim 3 Under 35 U.S.C. § 102

Claim 3 is rejected under 35 U.S.C. § 102(b) as being anticipated by USP No. 6,091,629 to Osada. Applicants respectfully traverse this rejection for at least the following reasons.

Claim 3, as amended, recites in-part a semiconductor device, wherein the bit line is connected to the same data line via the read column selection switch and the write column selection, separately.

In accordance with one exemplary embodiment of the present invention, the data transfer circuit includes a column selection switch having a read column selection switch Qn6 and a write column selection switch Qn5 for turning ON/OFF the connection between the data line DL and the bit line BL, wherein the bit line BL is connected to the data line DL via the read column selection switch Qn6, and via the write column selection switch Qn5, separately. As a result, the present invention advantageously prevents data corruption and misreading in a semiconductor memory device.

Turning to the cited prior art, at a minimum, Osada is silent with regard to connecting the bit line LBL to the same data line via the P-channel MOS transistor MP3 and the N-channel MOS transistor MN5, separately. In direct contrast, Osada discloses that the bit line LBL is connected to the read global bit line RGBL (alleged data line) via the P-channel MOS transistor MP3 (alleged read column selection switch), and to the write global bit line WGBL via the N-channel MOS transistor MN5 (alleged write column selection switch). In other words, Osada specifically discloses connecting the bit line LBL to the read global bit line RGBL via the P-channel MOS transistor MP3, and to the write global bit line WGBL via the N-channel MOS transistor MN5. As such, the data line (i.e., RGBL) to which the P-channel MOS transistor MP3 is connected and the data line (i.e., WGBL) to which the N-channel MOS transistor MN5 is connected are **not** the **same** data line. For the foregoing reasons, Osada does not disclose or suggest a semiconductor device, wherein the bit line is connected to the same data line via the read column selection switch and the write column selection, separately, as recited by amended claim 3.

Furthermore, it does not appear that Osada discloses or suggests the claim elements recited by new claim 9. Thus, it is respectfully submitted that new claim 9 is patentably distinct over the cited prior art.

Accordingly, as anticipation under 35 U.S.C. § 102 requires that each element of the claim in issue be found, either expressly described or under principles of inherency, in a single prior art reference, *Kalman v. Kimberly-Clark Corp., 713 F.2d 760, 218 USPQ 781 (Fed. Cir. 1983)*, and at a minimum, Osada fails to disclose or suggest the foregoing claim elements, it is clear that Osada does not anticipate claim 3 or any of the claims dependent thereon.

IV. All Dependent Claims Are Allowable Because The Independent Claims From Which They Depend Are Allowable

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co., 819 F.2d at 1100, 1108 (Fed. Cir. 1987)*. Accordingly, as independent claims 3 and 9 are patentable for the reasons set forth above, it is respectfully submitted that all claims dependent thereon are also in condition for allowance.

Accordingly, it is respectfully submitted that the rejection of claim 3 under 35 U.S.C. § 102 has been overcome.

V. Conclusion

Accordingly, it is urged that the application is in condition for allowance, an indication of which is respectfully solicited.

If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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Date: December 20, 2004